



High Efficiency Fast Response, 2A, 22V Input Synchronous Step Down Regulator

General Description

CS7120R develops high efficiency synchronous step-down DC-DC converter capable of delivering 2A load current . CS7120R operates over a wide input voltage range from 4.5V to 22V and integrates main switch and synchronous switch with very low RDS(ON) to minimize the conduction loss.

CS7120R adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates under heavy load conditions to minimize the size of inductor and capacitor.

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom): 145/135 m Ω
- 4.5-22V input voltage range
- 2A load current capability
- Instant PWM architecture to achieve fast transient responses Internal softstart limits the inrush current
- 2% 0.6V reference
- RoHS Compliant and Halogen Free
- Compact package: SOT23-6

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Package

- SOT23-6

Typical Applications

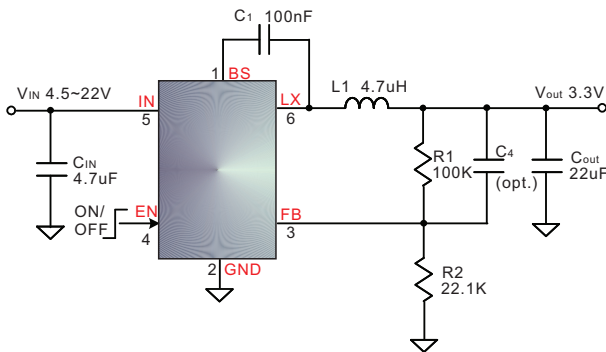


Figure1.Schematic Diagram

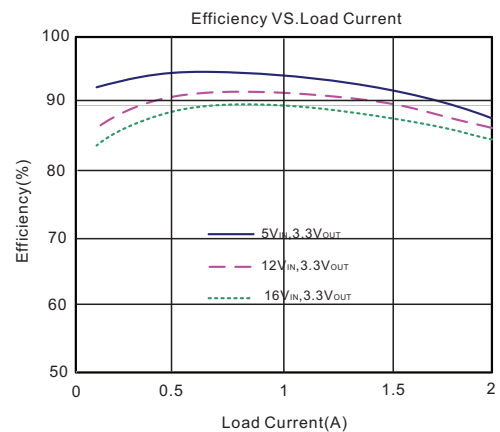
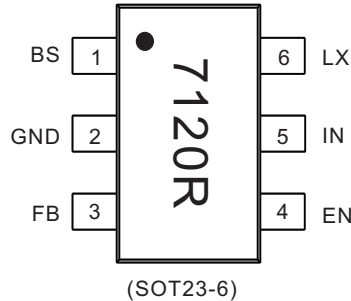


Figure2.Efficiency Figure



PIN Configuration and Functions



| NO | NAME | I/O | DESCRIPTION |
|----|------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | BS | I | Boot-Strap Pin. Supply high side gate driver. Decouple this pin to LX pin with 0.1 uF ceramic cap. |
| 2 | GND | P | Ground pin |
| 3 | FB | I | Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{out}=0.6*(I+R1/R2)$ |
| 4 | EN | I | Enable control. Pull high to turn on. Do not float. |
| 5 | IN | I | Input pin. Decouple this pin to GND pin with at least 1uF ceramic cap |
| 6 | LX | O | Inductor pin. Connect this pin to the switching node of inductor |

Absolute Maximum Ratings (Note 1)

| | |
|-----------------------------------------|----------------|
| Supply Input Voltage | -----23V |
| LX, EN Voltage | -----IN + 0.3V |
| FB, BS-LX Voltage | -----4V |
| Power Dissipation, PD@ TA= 25°C SOT23-6 | -----0.6W |

Package Thermal Resistance (Note 2)

| | |
|---------------------------------------|----------------------|
| θ_{JA} | -----170°C/W |
| θ_{JC} | -----130°C/W |
| Junction Temperature Range | -----125°C |
| Lead Temperature (Soldering, 10 sec.) | -----260°C |
| Storage Temperature Range | ----- -65°C to 150°C |

Package Thermal Resistance (Note 3)

| | |
|----------------------------|----------------------|
| Supply Input Voltage | -----4.5V to 22V |
| Junction Temperature Range | ----- -40°C to 125°C |
| Ambient Temperature Range | ----- -40°C to 85°C |

Order Information

| Device | Package | Making | Reel Size | Tape Width | Quantity |
|---------|----------|--------|-----------|------------|----------|
| CS7120R | SOT23L-6 | | 7" | 8mm | 3000 |



Electrical Characteristics

($V_{IN}=12V$, $V_{OUT} = 1.2V$, $L = 25\mu H$, $C_{OUT}=10\mu F$, $T_A=25^\circ C$, $I_{OUT} = 1A$ unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------------|-------------------|--------------------------------------------|-------|-------|-------|------------|
| Input Voltage Range | V_{IN} | | 4.5 | | 22 | V |
| Quiescent Current | I_Q | $I_{OUT}=0$, $V_{FB}=V_{REF}\times 105\%$ | | 0.1 | | μA |
| Shutdown Current | I_{SHDN} | EN=0 | | 5 | 10 | μA |
| Feedback Reference Voltage | V_{REF} | | 0.588 | 0.6 | 0.612 | V |
| FB Input Current | I_{FB} | $V_{FB}=V_{IN}$ | -50 | | 50 | nA |
| Top FET RON | $R_{DS(ON)1}$ | | | 0.145 | | Ω |
| Bottom FET RON | $R_{DS(ON)2}$ | | | 0.135 | | Ω |
| TOP FET Peak Current Limit | $I_{LIM, TOP}$ | | | | 3.6 | A |
| Bottom FET Valley Current Limit | $I_{LIM, BOTTOM}$ | | 2 | | | A |
| EN Rising Threshold | V_{ENH} | | 1.5 | | | V |
| EN Falling Threshold | V_{ENL} | | | | 0.4 | V |
| Input UVLO Threshold | V_{UVLO} | | | | 4.5 | V |
| Switching Frequency | F_{SW} | | | 500 | | kHz |
| Min ON Time | | | | 50 | | ns |
| Min Off Time | | | | 100 | | ns |
| Soft-start Time | t_{SS} | | | 800 | | us |
| Thermal Shutdown Temperature | T_{SD} | | | 150 | | $^\circ C$ |
| Thermal Shutdown Hysteresis | T_{HYS} | | | 15 | | $^\circ C$ |

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

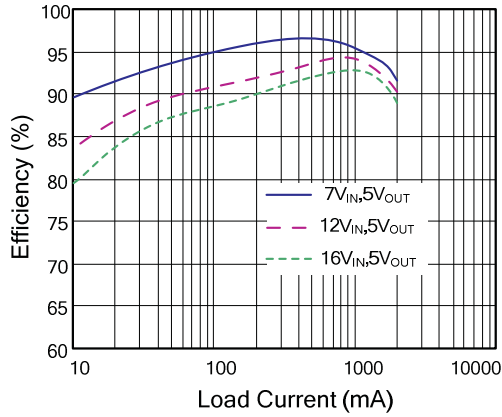
Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Pin 2 of SOT-23-6 packages is the case position for θ_{JC} measurement

Note 3: The device is not guaranteed to function outside its operating conditions.

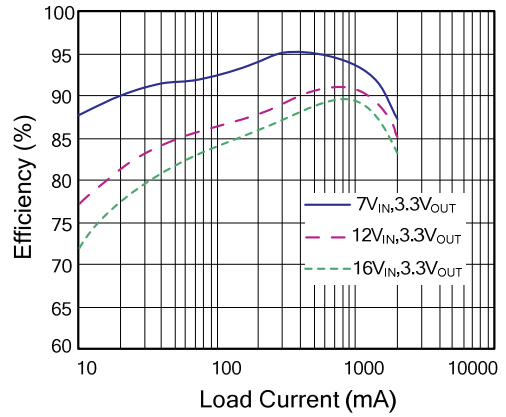


TYPICAL CHARACTERISTICS

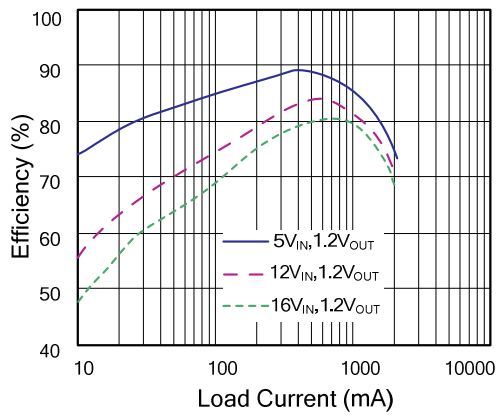
Efficiency vs. Load Current



Efficiency vs. Load Current

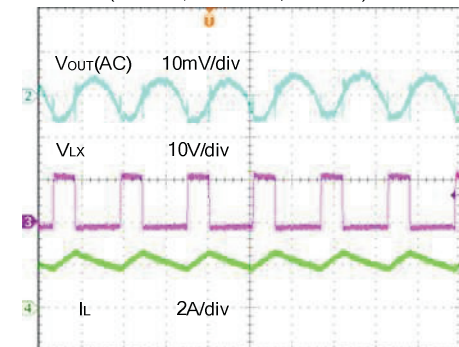


Efficiency vs. Load Current



Output Ripple

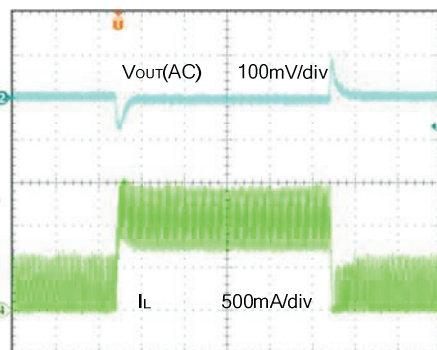
(V_{IN}=12V, V_{OUT}=3.3V, I_{LOAD}=2A)



Time (1μs/div)

Load Transient

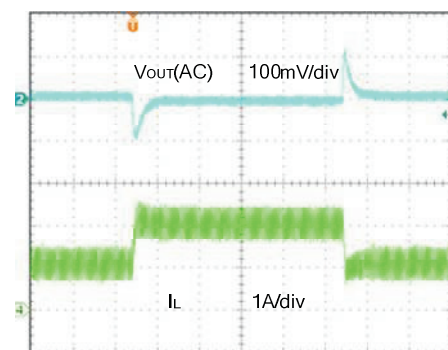
(V_{IN}=12V, V_{OUT}=3.3V, I_{LOAD}=0.2-1A)



Time 40μs/div

Load Transient

(V_{IN}=12V, V_{OUT}=3.3V, I_{LOAD}=1-2A)



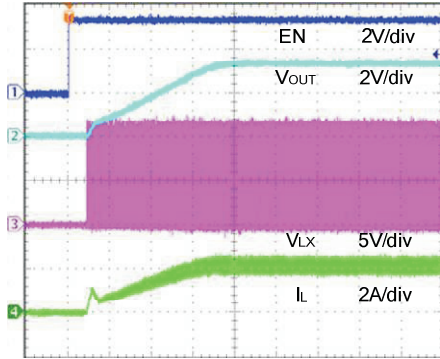
Time 40μs/div



TYPICAL CHARACTERISTICS

Startup

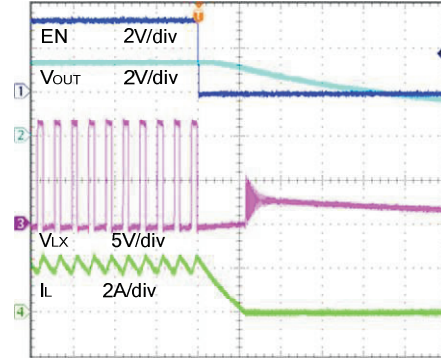
($V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{LOAD}=2A$)



Time (100us/div)

Shutdown

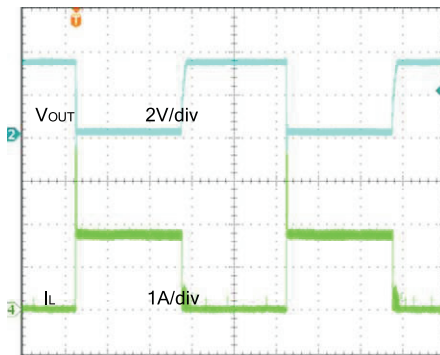
($V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{LOAD}=2A$)



Time (4us/div)

Short Circuit Protection

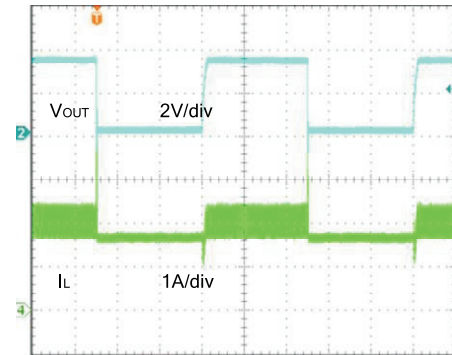
($V_{IN}=12V$, $V_{OUT}=3.3V$, Open to Short)



Time (2ms/div)

Short Circuit Protection

($V_{IN}=12V$, $V_{OUT}=3.3V$, 2A to Short)



Time (2ms/div)



Operation

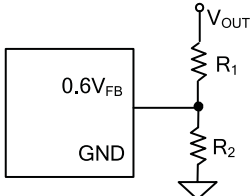
CS7120R is a synchronous buck regulator ic that integrates the PWM control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low Rds(on) power switches and proprietary PWM control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint CS7120R provides protection functions such as cycle by cycle current limiting and thermal shutdown protection. CS7120R will sense the output voltage conditions for the fault protection.

Applications Information

Because of the high integration in the CS7120R IC, the application circuit based on this regulator IC is rather simple. Only input capacitor Cin output capacitor Cout, output inductor L and feedback resistors (R1 and R2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R1 and R2:

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If Vout is 3.3V, R1=100k is chosen, then using following equation, R2 can be calculated to be 22.1k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1$$


Input capacitor CIN :

The ripple current through input capacitor is calculated as :

$$I_{CIN_RMS} = I_{OUT} \cdot \sqrt{D(1-D)}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins. In this case, a 4.7uF low ESR ceramic capacitor is recommended.

Output capacitor COUT:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 22uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor. (1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

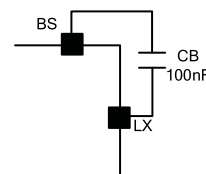
where Fsw is the switching frequency and Iout,MAX is the maximum load current. The CS7120R regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly the calculation value without significantly impacting the performance. (2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

(3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR < 50mΩ to achieve a good overall efficiency.

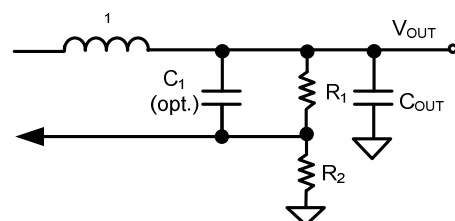
External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSFET. A 100nF low BSR ceramic capacitor connected between BS pin and LX pin is recommended.



Load Transient Considerations:

The CS7120R regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.





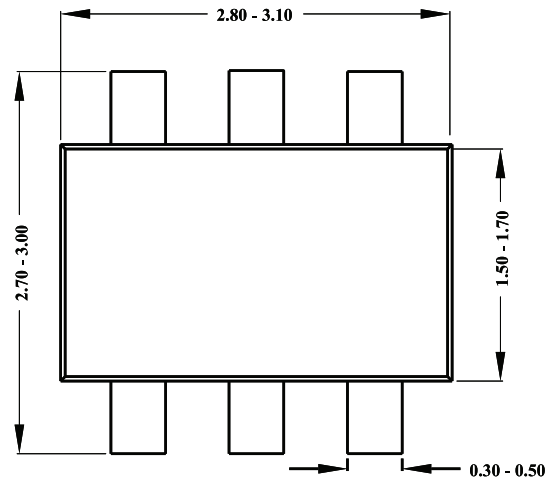
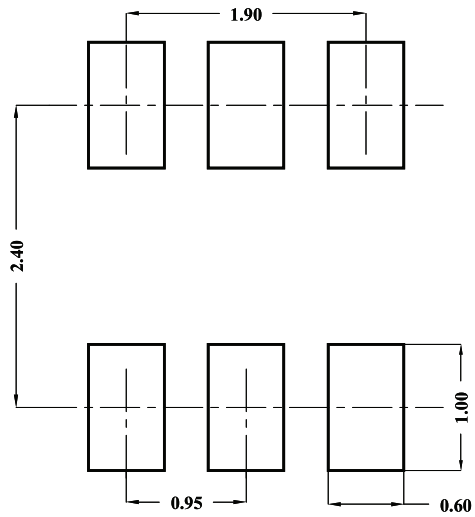
Layout Design:

The layout design of CS7120R regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC: C_{IN}, L, R1 and R2.

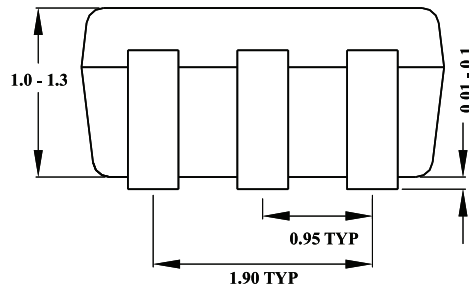
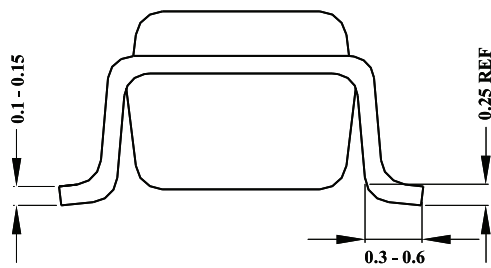
- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- 2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.
- 3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
- 4) The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.
- 5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.



SOT23-6L Package Outline & PCB layout



Recommended Pad Layout



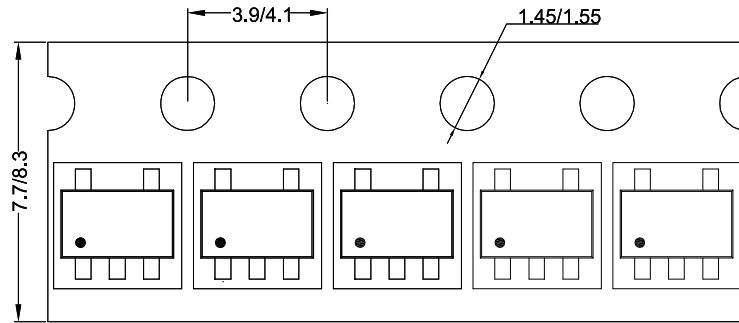
Notes: All dimension in MM
All dimension don't not include mold flash & metal burr



Taping & Reel Specification

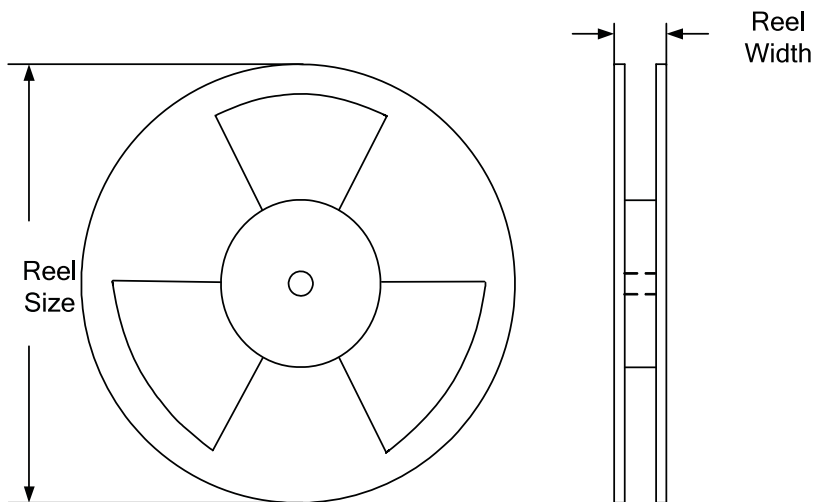
1. Taping orientation

SOT23-6



Feeding direction →

2. Carrier Tape & Reel specification for packages



| Package types | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Reel width(mm) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---------------|-----------------|------------------|------------------|----------------|--------------------|--------------------|--------------|
| SOT23-6 | 8 | 4 | 7" | 8.4 | 280 | 160 | 3000 |